IN THE CLAIMS:

Please amend the claims as follows:

1. (Currently amended) A method of manufacturing a semiconductor device said method forming metal wirings of a ~~predetermined~~ pattern connected through a conduction path to a control electrode on an insulating layer formed on a substrate, said method comprising ~~the steps of~~:

forming a metal film;

forming, on said metal film, a hard mask with a film thickness of at least 150 nm but not greater than 300 nm, said hard mask containing a silicon ~~system~~ inorganic insulating film, and said hard mask having said ~~predetermined~~ pattern; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said ~~predetermined~~ pattern;

wherein, in said step of forming said metal wiring, the amount of electric charge in said metal film is decreased to reduce the occurrence of the breakdown and deterioration, caused by said electric charge flowing into said control electrode, of said insulating layer.

2. (Original) A method of manufacturing a semiconductor device according to claim 1, wherein said hard mask is made of silicon oxide.

3. (Original) A method of manufacturing a semiconductor device according to claim 1 or 2, wherein said metal film is at least one of an Al film and an Al alloy film.

4. (Original) A method of manufacturing a semiconductor device according to claim 1 or 2, wherein said metal film is at least one of a tungsten film and a copper alloy film.

5. (Currently amended) A method of manufacturing a semiconductor device according to claim 1 ~~any one of claims 1 to 4~~, wherein said hard mask has a film thickness of at least 180 nm but not greater than 230 nm.

6. (Currently amended) A method of manufacturing a semiconductor device according to claim 1 ~~any one of claims 1 to 5~~, wherein a barrier metal film is formed.

7. (Currently amended) A method of manufacturing a semiconductor device according to claim 6, further comprising ~~the step of~~ etching said barrier metal film by use of said hard mask.

8. (Currently amended) A method of manufacturing a semiconductor device according to claim 1 ~~anyone of claims 1 to 7~~, wherein an antireflection film is provided between said metal film and said hard mask.

9. (Currently amended) A method of manufacturing a semiconductor device according to claim 8, further comprising ~~the step of~~ etching said antireflection film by use of said hard mask.

10. (Original) A method of manufacturing a semiconductor device according to claim 1, wherein said etching gas contains Cl.

11. (Currently amended) A method of manufacturing a semiconductor device having metal wirings of a ~~predetermined~~ pattern, said method comprising ~~the steps of~~:

forming, on an insulating layer, a control electrode for a metal-insulator-semiconductor type device;

forming a metal film connected through a conduction path to said control electrode;

forming, on said metal film, a hard. mask with a film thickness of at least 150 nm but not greater than 300 nm, said hard mask having said ~~predetermined~~ pattern and containing a silicon ~~type~~ inorganic insulating film; and

etching said metal film with said hard mask by use of an etching gas to form metal wiring of said ~~predetermined~~ pattern.

12. (Currently amended) A method of manufacturing a semiconductor device according to claim 11, further comprising ~~the step of~~ forming said insulating film prior to forming said control electrode on said insulating layer.

13. (Currently amended) A method of manufacturing a semiconductor device according to claim 11 or 12, further comprising ~~the step of~~ forming a source and a drain for said metal-insulator-semiconductor ~~type~~ device.

14. (Currently amended) A method of manufacturing a semiconductor device according to claim 11 ~~any one of claims 11 to 13~~, wherein said hard mask is made of silicon oxide.

15. (Currently amended) A method of manufacturing a semiconductor device according to claim 11 ~~any one of claims 11 to 14~~, wherein said hard mask has a film thickness of at least 180 nm but not greater than 230 nm.

16. (Currently amended) A method of manufacturing a semiconductor device according to claim 11 ~~any one of claims 11 to 15~~, further comprising ~~the steps of~~:

forming a barrier metal film prior to forming said metal film; and

etching said barrier metal film by use of said hard mask.

17. (Currently amended) A method of manufacturing a semiconductor device according to claim 11 ~~any one of claims 11 to 16~~, further comprising ~~the steps of~~:

forming an antireflection film on said metal film prior to forming said hard mask on said metal film; and

etching said antireflection film by use of said hard mask.

18. (Currently amended) A semiconductor device comprising:

a substrate;

a MIS type device having an electrode provided on an insulating film between said electrode and said substrate;

a metal wiring layer provided on said MIS type device by way of an interlayer insulating film, said metal wiring layer having a ~~predetermined~~ pattern; and

a hard mask, provided on said metal wiring layer, having a ~~predetermined~~ pattern identical to that of said metal wiring layer;

wherein said metal wiring layer is electrically connected to said electrode of said MIS type device.

19. (Currently amended) A semiconductor device comprising:

a substrate;

a MIS type transistor having a source and a drain provided on the substrate; and a control electrode for controlling a current flowing between said source and drain, said control electrode being provided on an insulating film, said insulating film being provided between said control electrode and said substrate;

a metal wiring layer provided on said MIS type transistor by way of an interlaver insulating film, said metal wiring layer having a ~~predetermined~~ pattern; and

a hard mask, provided on said metal wiring layer, having a ~~predetermined~~ pattern identical to that of said metal wiring layer;

wherein said metal wiring layer ~~being~~ is electrically connected to said control electrode of said MIS type transistor.

20. (Original) A semiconductor device according to claim 19, wherein said MIS type field-effect transistor is a MOS type field-effect transistor.